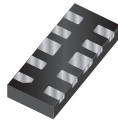


CTLTVS5-4**SURFACE MOUNT SILICON
LOW CAPACITANCE
QUAD TVS/DIODE ARRAY**www.centrasemi.com**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLTVS5-4 is a 4-line TVS/Diode array packaged in a TLM1031 surface mount case. With its ultra low capacitance, this device was designed to protect four high speed data or transmission lines from over-voltage transients and ESD damage.

MARKING CODE: CTL5**TLM1031 CASE****APPLICATIONS:**

- USB 3.0 Power and Data Line Protection
- HDMI Interface Protection
- Tablets, Monitors, Displays, Smart Phones
- Ethernet Ports

FEATURES:

- Low capacitance
- Low clamping voltage
- Protects four I/O lines

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Peak Pulse Current (8x20 μs)
 Peak Power Dissipation (8x20 μs)
 Electrical Fast Transient (IEC 61000-4-4) (5x50ns)
 ESD Voltage (IEC 61000-4-2, Air)
 ESD Voltage (IEC 61000-4-2, Contact)
 Operating and Storage Junction Temperature

SYMBOL

I_{PP} 2.5
 P_{PK} 32.5
 EFT 40
 V_{ESD} 15
 V_{ESD} 8.0
 T_J, T_{stg} -55 to +150

UNITS

A
 W
 A
 kV
 kV
 $^\circ\text{C}$

ELECTRICAL CHARACTERISTICS PER DIODE: ($T_A=25^\circ\text{C}$)

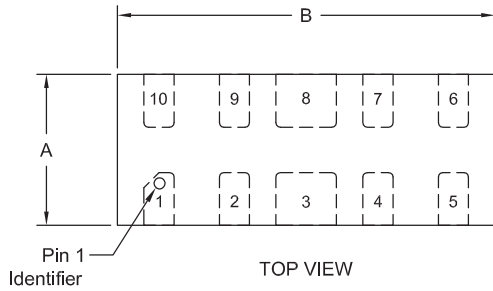
Maximum Reverse Stand-off Voltage V_{RWM}	Reverse Breakdown Voltage I/O to GND $V_Z @ 1.0\text{mA}$		Maximum Reverse Leakage Current I/O to GND $I_R @ V_{RWM}$	Maximum Clamping Voltage I/O to GND (8x20 μs) $V_C @ I_{PP}$		Typical TLP Clamping Voltage (Note 1) $V_{CL} @ I_{PP}$		Typical Dynamic Resistance (Note 1) R_{DYN}	Maximum Off State Junction Capacitance ($V_R=0, f=1.0\text{MHz}$)	
	MIN V	MAX V		V	A	V	A		I/O to GND	I/O to I/O
									C_J	C_J
V			μA	V	A	V	A	Ω	pF	pF
5.0	6.0	9.0	1.0	12	1.0	12	4.0	0.5	0.8	0.4
				13	2.5	14	8.0			

Note 1: Transmission Line Pulse (TLP) conditions: $Z_0=50\Omega, t_p=100\text{ns}$

CTLTVS5-4
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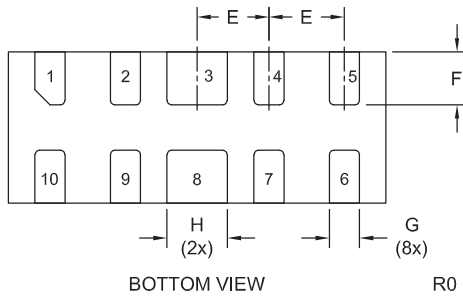
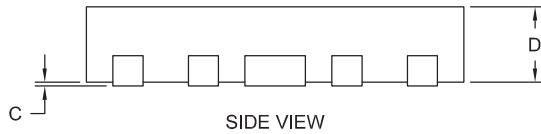


TLM1031 CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.041	0.95	1.05
B	0.096	0.100	2.45	2.55
C	0.000	0.002	0.00	0.05
D	0.018	0.022	0.45	0.55
E	0.020		0.50	
F	0.012	0.016	0.30	0.40
G	0.006	0.010	0.15	0.25
H	0.014	0.018	0.35	0.45

TLM1031 (REV:R0)

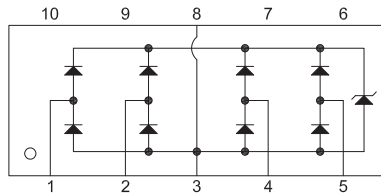


LEAD CODE:

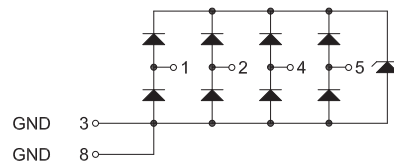
- 1) I/O
- 2) I/O
- 3) Ground
- 4) I/O
- 5) I/O
- 6) N/C
- 7) N/C
- 8) Ground
- 9) N/C
- 10) N/C

MARKING CODE: CTL5

PIN CONFIGURATION



SCHEMATIC



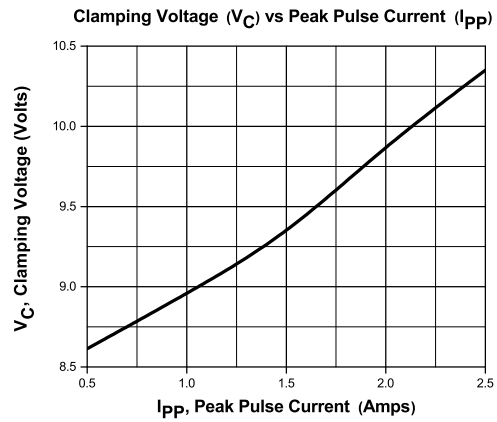
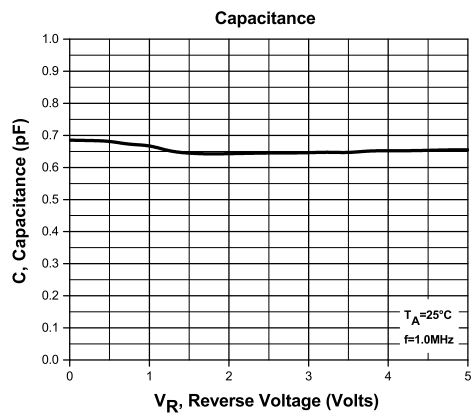
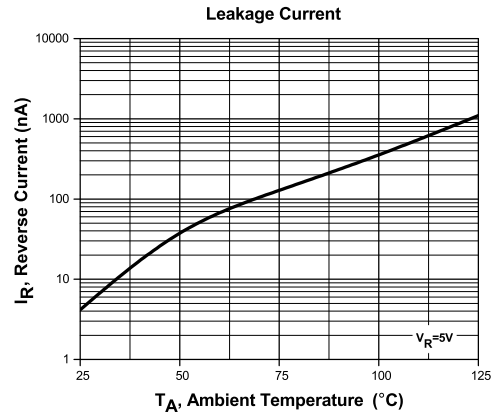
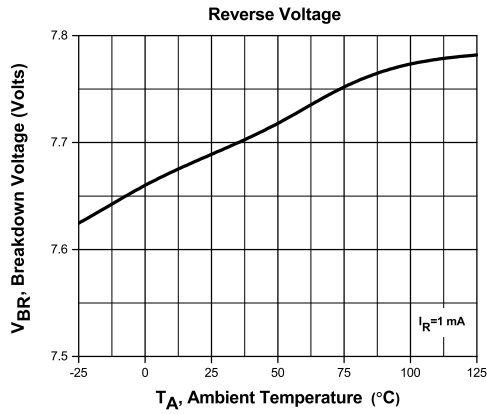
R4 (4-September 2015)

CTLTVS5-4

SURFACE MOUNT SILICON
LOW CAPACITANCE
QUAD TVS/DIODE ARRAY



TYPICAL ELECTRICAL CHARACTERISTICS



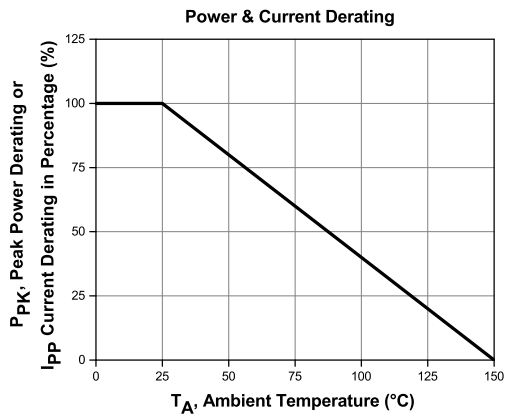
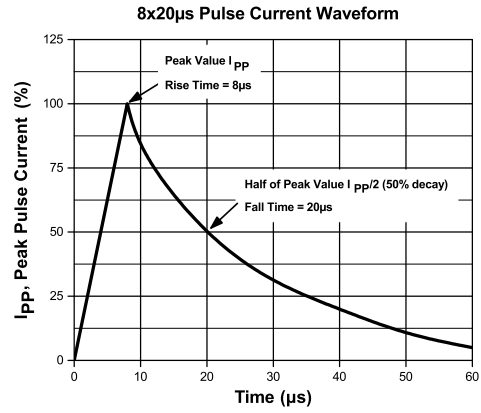
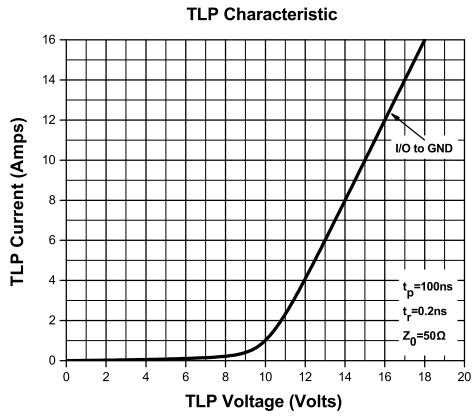
R4 (4-September 2015)

CTLTVS5-4

SURFACE MOUNT SILICON
LOW CAPACITANCE
QUAD TVS/DIODE ARRAY



TYPICAL ELECTRICAL CHARACTERISTICS



R4 (4-September 2015)

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

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